Department of Electrical and Computer Engineering

EEL 3712L – Logic Design I Lab
Fall 2022

Instructor	:	Dr. Nonnarit O-larnnithipong
Office Hours	:	by appointment Monday & Wednesday 11:00 am - 12:30 pm
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Class Time	:	Online
Website	:	Course content is available through FIU Canvas

Catalog Description:
Laboratory experiments, using gates, combinational networks, SSI, MSI, LSI. Sequential logic design. (1 Credit)

Reference Textbook: Open source materials are used as instruction materials

Course Objectives:
Through successful completion of the course, the student will be able to:

Develop truth tables.
Design combinational and sequential logic circuits using Xilinx Vivado
Implement their design on to the target FPGA platform.
Verify the characteristics of logic gates and combinational logic circuits.

Topic Covered:

1. AND Gates & OR Gates
2. Inverting Logic: NOT, NAND, & NOR
3. Boolean Laws & Rules and DeMorgan's Thoerem
4. XOR and XNOR Gates with Applications
5. Use of XOR/XNOR Gates to Generate & Check Parity
6. Binary Adders
7. Decoders & Applications
8. Encoder & Application to a 7-Segment Display Driver
9. Multiplexer & De-Multiplexer

ABET Relationship of course to program outcomes:

- ☒ 1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.
- ☒ 2. an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.
- ☒ 3. an ability to communicate effectively with a range of audiences.
- ☐ 4. an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts.
- ☐ 5. an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives.
- ☒ 6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.
- ☐ 7. an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

Grading Scale:		
A	95-100	"Florida International University is a community dedicated to generating and imparting knowledge through excellent teaching and research, the rigorous and respectful exchange of ideas, and community service. All students should respect the right of others to have an equitable opportunity to learn and honestly to demonstrate the quality of their learning. Therefore, all students are expected to adhere to a standard of academic conduct, which demonstrates respect for themselves, their fellow students, and the educational mission of the University. All students are deemed by the University to understand that if they are found responsible for academic misconduct, they will be subject to the Academic Misconduct procedures and sanctions, as outlined in the Student Handbook."
A-	90-94	
B+	87-89	
B	83-86	
B-	80-82	
C+	77-79	
C	70-76	
D	60-69	
F	< 60	

Department Regulations Concerning Incomplete Grades

To qualify for an Incomplete, a student:

1. Must contact (e.g., phone, email, etc.) the instructor or secretary before or during missed portion of class
2. Must be passing the course prior to that part of the course that is not completed
3. Must make up the incomplete work through the instructor of the course
4. Must see the Instructor. All missed work must be finished before last two weeks of the following term.

Policies:

1. **Academic Misconduct:** For work submitted, it is expected that each student will submit their own original work. Any evidence of duplication, cheating or plagiarism will result at least a failing grade (F) for the course. Please DO NOT SHARE your assignments/classwork with other students. If the evidence of duplication is found, 0 point will be given, no exception.
2. **Lab Report:** Fill out the results in the truth table(s), answer the questions at the end of the experiment, and include photos of functioning BASYS3 board within the report file. Submit the report in a single PDF file. Report submitted without photos of BASYS 3 board will automatically receive 0 point.
3. **Deadlines:** Work is due on the date and time specified. Late submissions will not be accepted. Participation and submission deadlines are absolute. (Only emergency medical situations or extenuating circumstances are excused with proper documentation.)
4. DO NOT submit work by email.
5. Instructor reserves right to change course materials or dates as necessary.

Course Requirements

Students are required to prepare the following lab equipment:

- Digilent BASYS 3 Artix-7 FPGA Trainer board
- Male micro USB to male USB-A cable that supports data transfer
- A computer running Windows 10 Operating System
- Xilinx Vivado Design Suite 2020.2 - HL WebPACK Edition

Grading Scale:

Topic	Percentage
Lab Reports	60%
Midterm Exam	20%
Final Exam	20%

Class Schedule:

Wk	Date	Content	Due Date
1	8/22 - 8/28	Module 0 | Course Introduction and Equipment Preparation	Electrical Safety Certificate Sun 8/28
2	8/29 - 9/4		
3	9/5 - 9/11	Module 1 | AND Gates & OR Gates	Sun 9/11
4	9/12 - 9/18	Module 2 | Inverting Logic: NOT, NAND, & NOR	Sun 9/18
5	9/19 - 9/25	Module 3 | Boolean Laws & Rules and DeMorgan's Theorem	Sun 9/25
6	9/26 - 10/2	Module 4 | XOR and XNOR Gates with Applications	Sun 10/2
7	10/3 - 10/9	**Midterm Exam** (Honorlock is required)	Sat 10/8
8	10/10 - 10/16	Module 5 | Use of XOR/XNOR Gates to Generate & Check Parity	Sun 10/16
9	10/17 - 10/23	Module 6 | Binary Adders	Sun 10/23
10	10/24 - 10/30	Module 7 | Decoders & Applications	Sun 10/30
11	10/31 - 11/6	Module 8 | Encoders & Application to a 7-Segment Display Driver	Sun 11/6
12	11/7 - 11/13	Module 9 | Multiplexers & De-Multiplexers	Sun 11/13
13	11/14 - 11/20	**Final Exam** (Honorlock is required)	Sat 11/19